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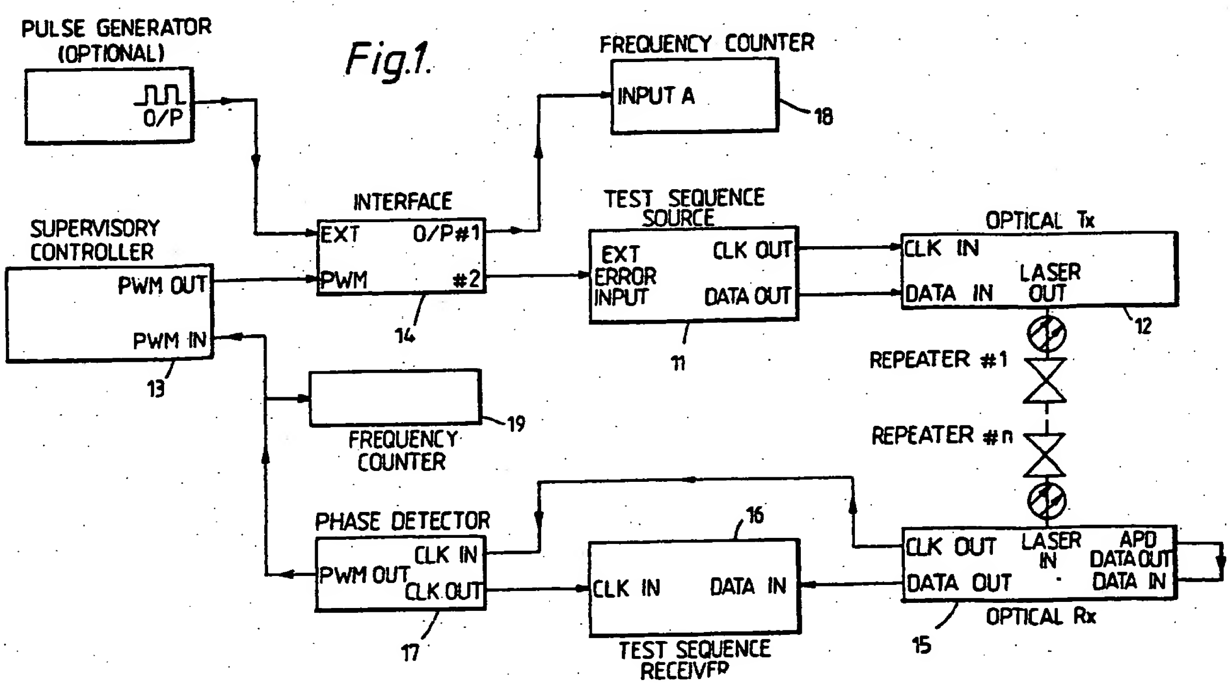
(54) Repeater supervision

(57) An arrangement for signalling to supervisory equipment in a repeater in a digital transmission system, the arrangement including means for generating a digital data test sequence comprising a plurality of multi-bit words each accompanied by a parity check bit, means for feeding said test sequence to the transmission systems at the system transmission rate, means for generating digital supervisory signals, means for imposing periodic inversions of bits of the test sequence in accordance with said supervisory signals, said supervisory signals modulating the imposed inversions.

Fig.1.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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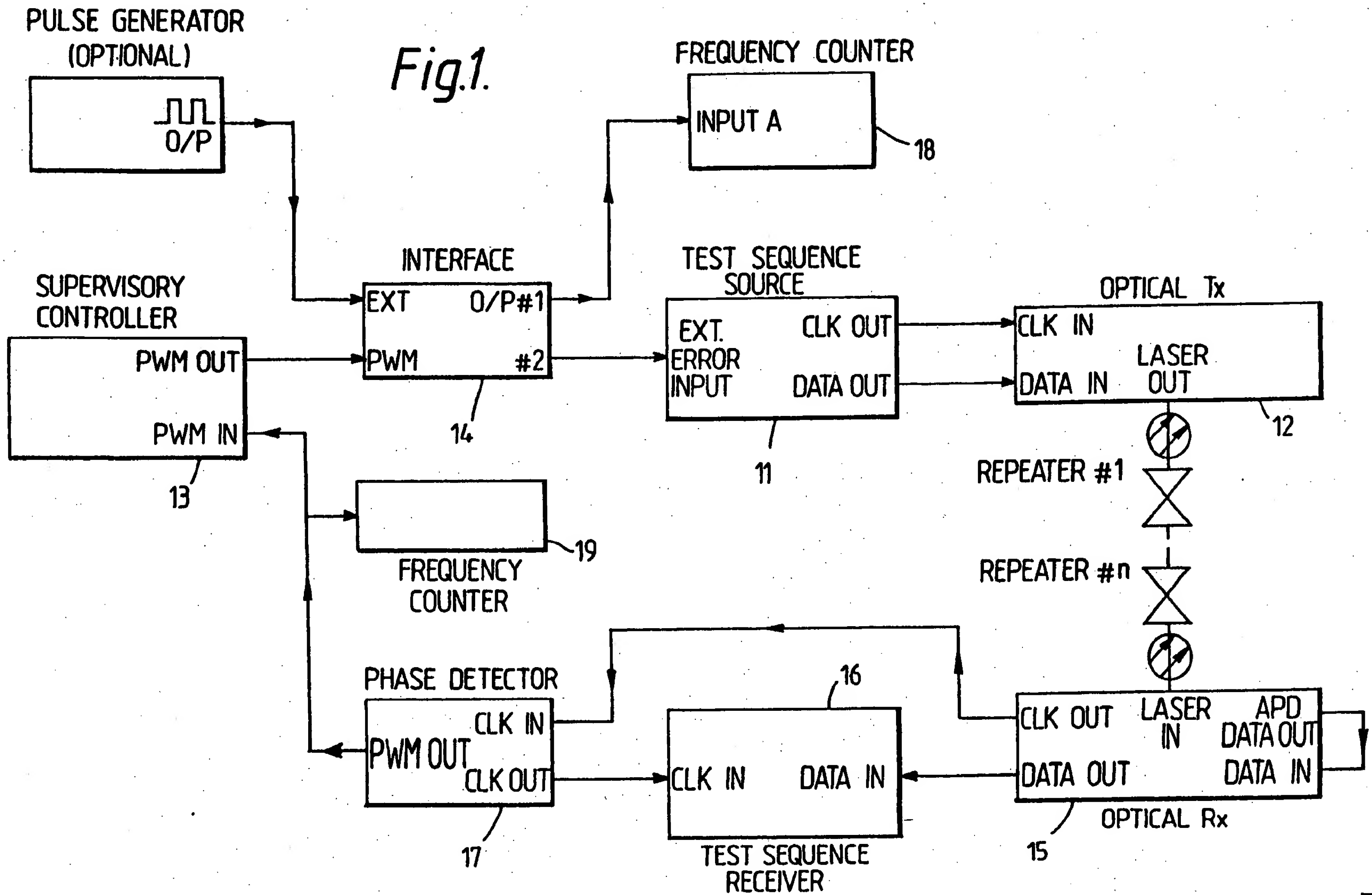
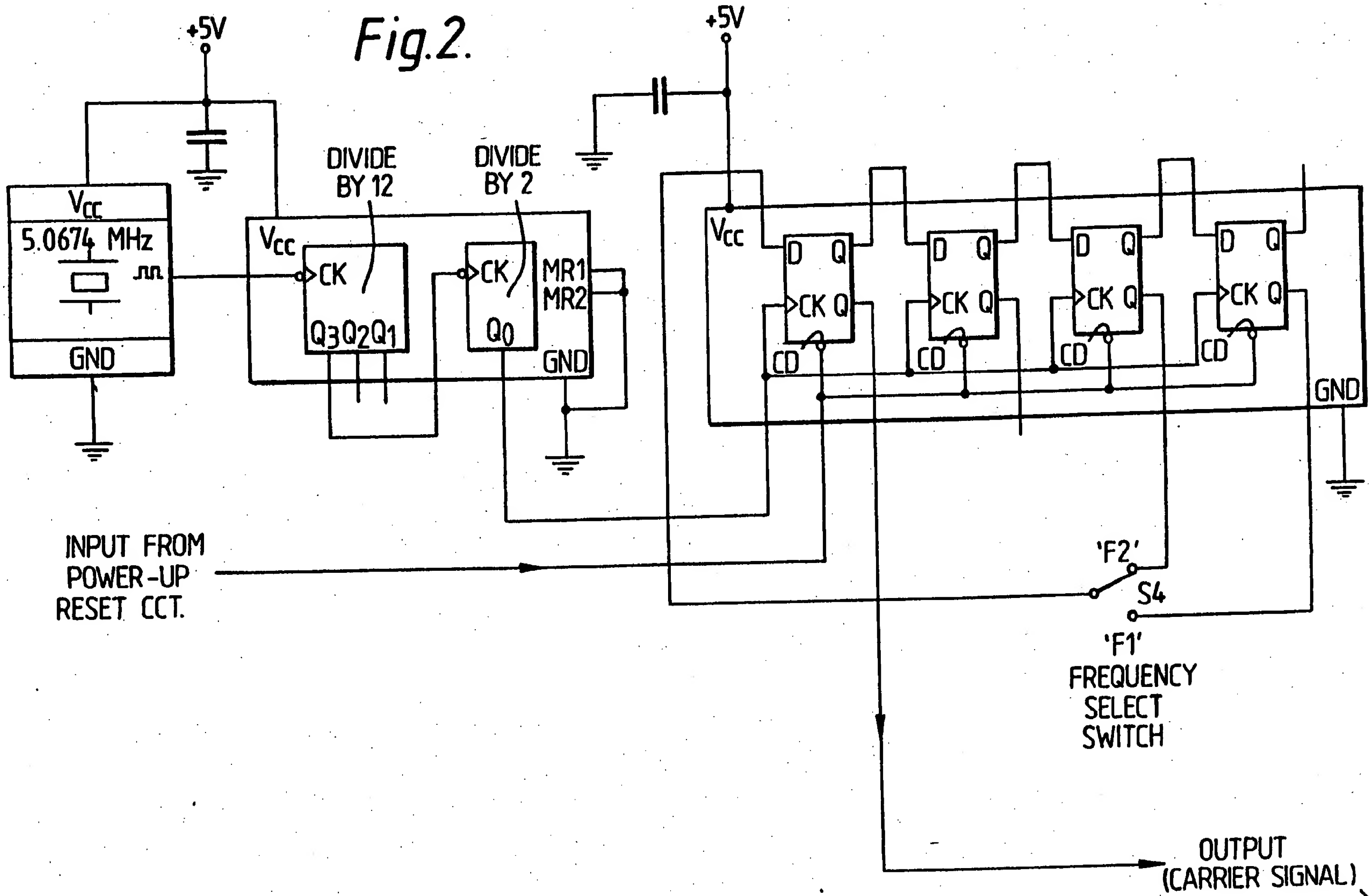
Fig.1.

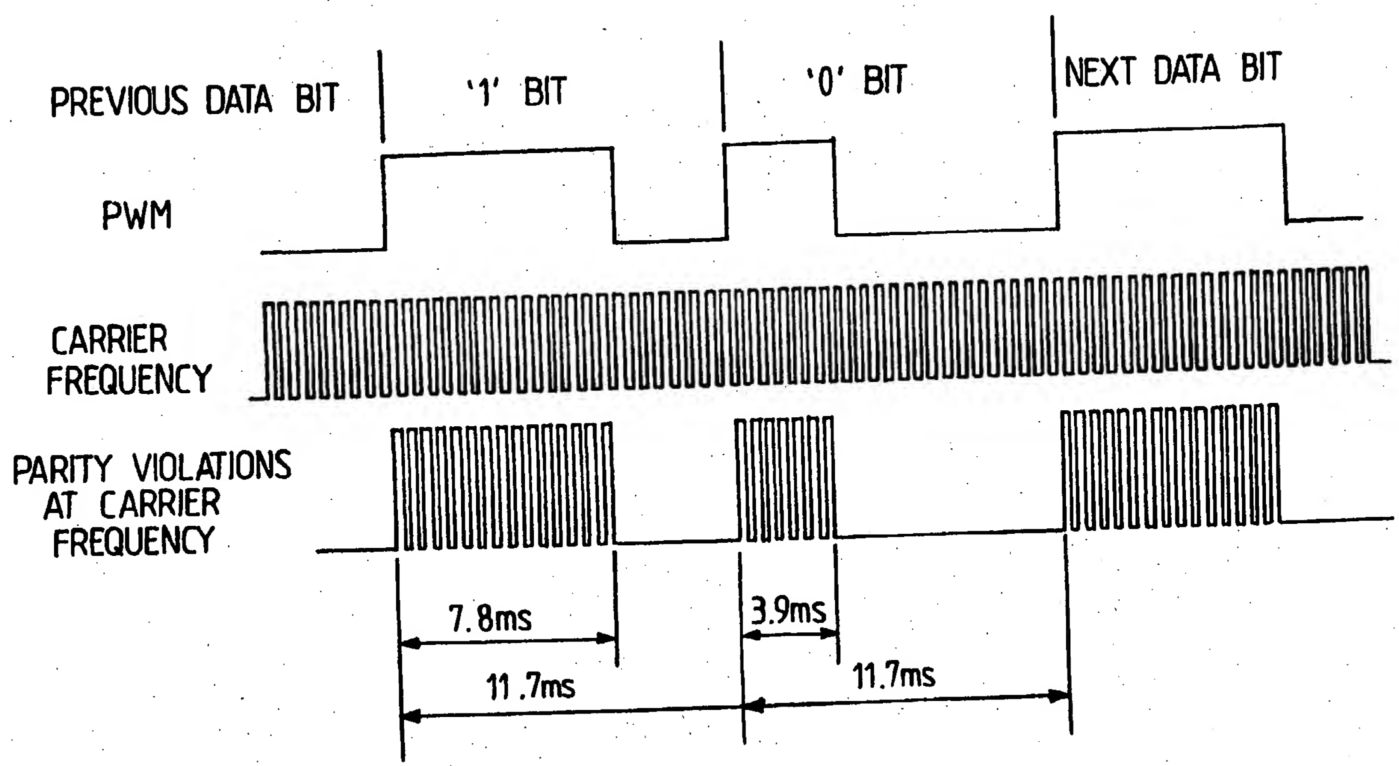


PULSE GENERATOR (OPTIONAL)
O/P
SUPERVISORY CONTROLLER
PWM OUT
PWM IN
13
INTERFACE
EXT
O/P#1
PWM
#2
14
FREQUENCY COUNTER
INPUT A
18
TEST SEQUENCE SOURCE
EXT. ERROR INPUT
CLK OUT
DATA OUT
11
OPTICAL Tx
CLK IN
DATA IN
LASER OUT
12
REPEATER #1
REPEATER #n
FREQUENCY COUNTER
19
PHASE DETECTOR
PWM OUT
CLK IN
CLK OUT
17
CLK IN
DATA IN
16
TEST SEQUENCE RECEIVER
CLK OUT
DATA OUT
LASER IN
APD DATA OUT
DATA IN
OPTICAL Rx
15

Fig.2.



+5V
Vcc
5.0674 MHz
GND
DIVIDE BY 12
DIVIDE BY 2
CK
Q3 Q2 Q1
Q0
MR1
MR2
+5V
Vcc
D Q
CK Q
CD
GND
INPUT FROM POWER-UP RESET CCT.
'F2'
S4
'F1'
FREQUENCY SELECT SWITCH
OUTPUT (CARRIER SIGNAL)


PREVIOUS DATA BIT
'1' BIT
'0' BIT
NEXT DATA BIT
PWM
CARRIER FREQUENCY
PARITY VIOLATIONS AT CARRIER FREQUENCY
7.8ms
3.9ms
11.7ms
11.7ms

Repeater Supervision

This invention relates to arrangements for digital supervision of repeaters in digital transmissions systems.

In the transatlantic submarine optical fibre system designated TAT-9 the repeater supervisory sub-system provides monitoring facilities which aid submerged equipment fault location. It also enables switching between redundant laser transmitters and between redundant paths, in response to signals from a terminal. All functions except loopback are available with the transmission system in service so that incipient failures can be detected.

Typically the line code used in the system is 24B1P. That is, for every 24 binary data bits transmitted to line, a 25th bit is added, such that the 25-bit word has even mark parity. At the receive terminal, the parity condition can be checked to see if an error has occurred in any 25-bit word. The parity bit will indicate if an error has occurred, but not its position in the word.

The receive terminal is able to identify the position of the parity bit within the data stream by rather complex circuitry, but in the repeater a simple method has been devised which allows errors to be

detected. Non return to zero (NRZ) data and clock are summed together to produce return to zero (RZ) pulses. These RZ pulses are passed through a divide-by-2 divider. For an even mark parity signal each word will generate even numbers of RZ pulses. Thus, provided there have been no errors, the output of the divider will always be in the same state at the time the parity bit has been processed. If the data bits are random, then the output for these bits will be random. Thus for 0 or 1 status at the output of the divider, there will be an average DC level with a small offset. The offset polarity will depend on the previous history. If a word with a single error is encountered, then there will be an odd number of pulses and hence the parity bit state will be reversed and so will the offset polarity. Provided no more errors occur the new offset state will be maintained. A low pass filter (LPF) is used to filter out high frequency components of the divider, and thus errors can be detected by noting the change in DC polarity at the output.

The arrangement just described can also be used to establish a communication channel as follows. If the integrity of the parity bits of the data is periodically violated at a slow rate at the terminal, then the offset at the output of the divider will follow these violations at the same slow rate. Periodic parity bit violation at the slow rate produces a tone which can be used as a carrier for supervisory commands.

In practice two different slow rates of signalling are used to provide two different tones, one for each direction of transmission.

The parity violations are affected intermittently so that the detected tone is modulated on and off at a predetermined pulse repetition frequency

(PRF). Information may then be coded onto this carrier system by pulse width modulating the bursts of tone. For example:-

'1' - Tone on 7.9mS off 3.9 mS

'0' - Tone on 3.9mS off 7.9 mS.

Commands are sent to the repeaters as words which contain information on repeater to be addressed and facility required.

According to the invention there is provided an arrangement for signalling to supervisory equipment in a repeater in a digital transmission system, the arrangement including means for generating a digital data test sequence comprising a plurality of multi-bit words each accompanied by a parity check bit, means for feeding said test sequence to the transmission system at the system transmission rate, means for generating digital supervisory signals, means for imposing periodic inversions of bits of the test sequence in accordance with said supervisory signals, said supervisory signals modulating the imposed inversions.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which:-

Fig. 1 is a block schematic illustration of a repeater supervision arrangement,

Fig. 2 is a schematic of a carrier signal generator,

Fig. 3 illustrates pulse width modulation of carrier tones.

In the arrangement of Fig. 1 a test sequence source 11 is set up to provide a digital data test sequence, for example a 2000 bit sequence in which every 24 bits is accompanied by a parity bit. Typically the test sequence source comprises a programmable shift register arrangement, the contents of which are read out as data under control of an internal clock, which also provides a clock output. The clock and data outputs are applied to an optical transmitter 12 which feeds the data as optical digital signals to the transmission system, e.g. a repeatered submarine optical fibre system.

To provide telemetry and other supervisory signalling to the system repeaters controlled sequences of periodically occurring errors are imposed on the test sequence.

The sequence of errors conform to a slow, pulse width modulated (PWM) digital coded data signal generated in supervisory controller 13. The PWM coded signals are applied to an interface circuit 14 where they control the output of a local clock source the frequency of which is such that it provides a signalling tone. This signalling tone is thus modulated in accordance with the PWM supervisory signalling code. Details of the tone modulation have been given above. The system optical receiver 15 feeds the received signalling data to a test sequence receiver 16. A clock derived from the received optical signals is fed to a phase detector 17 which provides a clock control for the test sequence receiver 16. The phase detector also provides a PWM output which carries telemetry and other signalling from the repeaters and feeds this PWM output to the supervisory controller 13.

As mentioned above, the system utilises two different tones for the two directions of data

transmission. Thus, depending on which end of the system the supervisory controller is situated the interface 14 will be required to produce one or other of the two tones for the supervisory signalling. For practical purposes it is desirable that the required tone be selected by simple switching from a single local oscillator. Fig. 2 shows such an arrangement. A crystal oscillator running at 5.0674 MHz feeds a divide-by-12 counter 21. After a further division by 2 the output is applied to a quad D-type flip-flop which acts as either a modulo 8 or a modulo 6 counter depending on selection of the appropriate flip-flop output via switch S4. Thus using switch S4 either frequency F1 = 52.785 kHz or frequency F2 = 70.381kHz is provided. The output carrier signal is fed via a further switch S3 to a PWM modulator operating in accordance with the required supervisory signalling code. Switch S3 is included to allow an external carrier signal from another source to be used instead of F1 or F2. It is to be noted that F1 and F2 are each in fact twice the tone frequency required in the repeaters. This is because, as noted above, the signals received in each repeater are initially passed through a divide-by-2 circuit.

To communicate with a repeater, deliberate parity violations are injected into the transmissions of the test sequence. This is achieved by causing a false parity bit to be sent after the appropriate 24-bit block of data. To send information to a regenerator the parity violations must be sent at a periodic rate. Data is therefore recognised in the repeater as pulse width modulated tones. Fig. 3 illustrates PWM modulation of the F1 and F2 carrier. Each PWM bit is 11.7ms in duration. A binary 1 is transmitted as 7.8ms of tone (carrier) followed by 3.9ms of silence (no carrier). A binary 0 is the inverse of the binary 1.

The PWM modulated signal output of the interface 14 is applied to the bit sequence source 11 and to a frequency counter 18 where the number of injected errors is counted to provide a monitoring facility. A similar counter 19 coupled to the PWM output of the phase detector 17 will count the errors received from the repeater(s). Comparison of the counts in counters 18 and 19 will indicate the satisfactory operation or otherwise of the system.

CLAIMS

1. An arrangement for signalling to supervisory equipment in a repeater in a digital transmission system, the arrangement including means for generating a digital data test sequence comprising a plurality of multi-bit words each accompanied by a parity check bit, means for feeding said test sequence to the transmission system at the system transmission rate, means for generating digital supervisory signals, means for imposing periodic inversions of bits of the test sequence in accordance with said supervisory signals, said supervisory signals modulating the imposed inversions.

2. An arrangement according to claim 1 wherein said digital supervisory signals are pulse width modulated signals.

3. An arrangement according to claim 1 or 2 including means for selectively generating at least two different rate clock signals, said periodic inversions of bits being imposed at the selected clock rate.

4. An arrangement according to claim 3 wherein the means for selectively generating alternative rate clock signals comprises a stable crystal oscillator, a first fixed divider circuit to which the oscillator is applied, a multiple flip-flop counter arrangement to which the divider circuit output is applied, and a selector switch the operation of which selects an output from one or other of the flip-flops in the counter.

5. An arrangement according to any preceding claim including a first frequency counter for counting the periodic violations imposed on the test sequence and a second like frequency counter for counting errors in test signals returned from the system.

6. A supervisory signalling arrangement for a repeatered digital transmission system substantially as described with reference to the accompanying drawings.

7. A method of signalling to supervisory equipment in a repeater in a digital transmission system, the method including the steps of generating a digital data test sequence comprising a plurality of multi-bit words each accompanied by a parity check bit, feeding said test sequence to the transmission system at the system transmission rate, generating digital supervisory signals, imposing periodic inversions of bits of the test sequence in accordance with said supervisory signals, said supervisory signals modulating the imposed inversions.

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